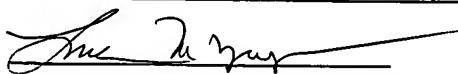


<b>FORM PTO-1449 U.S. Department of Commerce</b> Patent and Trademark Office  <b>LIST OF DOCUMENTS CITED BY APPLICANT</b>  (Use several sheets if necessary)				Attorney Docket Number 5646-114		Serial No. To Be Assigned  <div style="font-size: 1.2em;">10/663,624</div>	
				Applicants: Paul Murtagh			
				Filing Date: Concurrently Herewith <div style="font-size: 1.2em;">09/16/03</div>		Group <div style="font-size: 1.2em;">2816</div>	
U. S. PATENTS & PATENT APPLICATION PUBLICATIONS							
Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate	
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<b>FORM PTO-1449 U.S. Department of Commerce</b> <b>Patent and Trademark Office</b>  <b>LIST OF DOCUMENTS CITED BY APPLICANT</b>  (Use several sheets if necessary)		<b>Attorney Docket Number</b> 5646-114	<b>Serial No.</b> <b>To Be Assigned</b>  10/883, 624
		<b>Applicants:</b> Paul Murtagh	
		<b>Filing Date:</b> Concurrently Herewith 09/16/2000	<b>Group</b> 2816
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>			
	26	Moon et al., "An All-Analog Multiphase Delay-Locked Loop Using a Replica Delay Line for Wide-Range Operation and Low-Jitter Performance," IEEE Journal of Solid-State Circuits, Vol. 35, No. 3, March 2000	

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Attorney Docket Number  
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Serial No.  
10/663.624

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**Applicants: Paul Murtagh**

Filing Date: September 16 2003

Group  
2816

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[illegible]

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		Document Number	Date	Country	Class	Subclass	Translation Yes   No

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